

REMARKS

Claims 1-16 are pending in this application. Claims 1-16 stand rejected. By this Amendment, claims 1, 9, and 11 have been amended. Claims 4, 10, 15, and 16 have been canceled without prejudice. The amendments made to the claims do not alter the scope of these claims, nor have these amendments been made to define over the prior art. Rather, the amendments to the claims have been made to improve the form thereof. In light of the amendments and remarks set forth below, Applicants respectfully submit that each of the pending claims is in immediate condition for allowance.

Claim 1 includes a cryptoprocessor having a register memory. This register memory is physically disposed within the cryptoprocessor.

Furthermore, there is a volatile working memory, which on the one hand, consists of a part of the register memory from the cryptoprocessor, which is not assigned to operands due to the functionality of the register memory configuration unit. Naturally, this part is physically disposed within the cryptoprocessor.

Additionally, the volatile working memory includes an external working memory, which is physically disposed outside the cryptoprocessor.

Notably, at least a part of the register memory, which is of course, physically disposed within the cryptoprocessor, is mapped into the working memory, i.e. is accessible in a straightforward manner.

The address unit performs the addressing of the working memory, particularly the addressing of the register memory space belonging to the volatile working memory. Particularly, the address unit addresses the volatile working memory part residing within the cryptoprocessor in the same way as the external working memory, which is physically disposed outside the cryptoprocessor.

Due to the fact that the register memory part is mapped into the working memory, the address unit can access or address this register memory space in the same way as the external working memory.

Thus, any device connected to the processor as defined in claim 1, can access the part of the register memory physically disposed within the cryptoprocessor, in the same way as any working memory such as a dynamic RAM, or any other memory, as shown in Fig. 3 in item 30. Thus, in accordance with the present invention, when a certain part of the register memory is free, this is signaled by the register memory configuration unit. Thus, this part can be used by any other device by simply addressing this part within the cryptoprocessor as any working memory located outside the cryptoprocessor, such as a dynamic RAM, etc., which is indicated as "XRAM" in Fig. 2. In this regard, any device can use a part of the register memory located within the cryptoprocessor, the cryptoprocessor not needing this part of the register memory.

Amended claim 9 is similar to claim 1, but is not directed to a cryptoprocessor, but to a "peripheral device" which importantly, comprises an internal memory, as stated in the second paragraph of claim 9. Thus, any peripheral device having an internal memory is within the definition of this paragraph, but a peripheral device not having an internal memory is not in the definition of this paragraph of claim 9.

The reasoning behind claim 9 is that there can be a situation, in which the peripheral device has a certain amount of internal memory, but does not need the whole internal memory for a certain task. When this is the case, then the non-used part of the internal memory of the peripheral device is made available for other data, by access via an external bus, i.e. for usage of another device connected to the external bus.

Due to the fact that a part of the internal memory of the peripheral device not actually used by the peripheral device itself is mapped into the working memory, this part of the memory can be addressed by the inventive address unit.

Thus, the same advantage can be obtained, i.e. that any internal memory of a peripheral device which is currently not used by this peripheral device can be accessed by any other device via the address unit, since the non-used internal memory is mapped into the working memory, and since the non-used internal memory is addressed by the address unit not in a very specific way, but is addressed like a straightforward external working memory which is not included in an I/O device's internal memory.

Claims 15 stands rejected under 35 USC § 103 (a) as unpatentable over US6,026,485 (O'Connor), in view of US5,818,938 (Davis).

Fig. 1 in O'Connor illustrates a hardware processor 100 having a stack cache 155 and a stack management unit 150, including the stack cache 155 and some other elements, such as the stack control unit, etc.

Importantly, please also refer to the top of Fig. 1, illustrating a double-arrow which has the following language "to external memory". Thus, O'Connor illustrates an internal processor 100, which is connected to an external memory. Furthermore, please also note that in column 31, line 52 stating that: "stack cache 155 is a 64 entry 32 bit wide array of registers that is physically implemented as a register file in one embodiment."

The randomly accessible storage 810 (column 20, lines 9-10) is implemented via the stack cache 155 as stated in column 21, lines 8-11. Thus, we have the following situation in O'Connor:

There is a stack cache 155 in addition to the data cache 165, which are both located within the processor, and which are implemented as a register file, as illustrated in Fig. 8, item 810. There is, in addition, an external memory physically disposed outside the processor 100.

Regarding claim 1, O'Connor does not disclose the following:

a volatile working memory including an external working memory physically disposed outside the cryptoprocessor and the register memory space not assigned to operands, which is physically disposed within the cryptoprocessor.

Furthermore, O'Connor does not disclose that at least a part of the register memory, which is physically located within the cryptoprocessor is mapped into the working memory.

Furthermore, O'Connor does also not disclose an address unit operable to address the register memory space, not assigned to operands, which is physically located within the cryptoprocessor, in the same way as the external working memory.

Instead, O'Connor discloses a clearly separated "external memory", as shown in Fig. 1 and further discussed in column 13, lines 23-28. This external memory is completely separate from the internal register file memories of the stack cache 155 or the data cache 165.

Thus, the Examiner is not correct when he states that "at least part of the memory was mapped to a physically working memory" in the first two lines of section 4. It is possible that the Examiner completely overlooked the limitations in claim 1 that the external working memory is physically disposed outside the cryptoprocessor and the part of the register memory, which is mapped into the working memory is physically located within the cryptoprocessor.

Furthermore, the Examiner overlooked the limitation of the address unit, as defined in claim 1. This limitation is not at all mentioned in the Office Action under section 3.

Regarding US 5,808,939 (Davis), it is to be emphasized that this reference is completely silent about any usage of available memory in item 305 together with the memory in the main memory 310. Regarding the processing unit 605, please refer to column 5, lines 22-24. Regarding the processing unit 605, it is not mentioned that this processing unit includes a register memory part which is made available for other devices or which is addressed in the same way as the volatile memory element 615.

Thus, even when those skilled in the art would combine O'Connor and Davis, they would not arrive at a device having the inventive features of claim 15, being that the volatile working memory includes an external memory outside the cryptocoprocessor and a register memory space physically disposed within the cryptocoprocessor.

Furthermore, this combination would not result in the feature that at least a part of the register memory (physically located within the cryptocoprocessor) is mapped into the working memory.

Finally, this combination would not result in the inventive address unit operable to address the register memory's space not assigned to operands and physically located outside the cryptocoprocessor in the same way as the external working memory, physically located outside the cryptocoprocessor.

In view of this, new claim 1 is not rendered obvious by the combination of both references.

Claim 16 is not obvious in view of the cited references.

US patent No.4,777,589 (Boettner), hereinafter referred to as Boettner, discloses a direct input/output in a virtual memory system. There is, as shown in Fig. 1, a system memory and a plurality of I/O devices. Importantly, please refer to column 1, lines 29-33 saying that an I/O device has a register and saying that each register within an I/O device is associated with an address within the address space. Thus, a read or write to an address within an I/O device's address space results in a read or a write to a register within the I/O device associated with the specific address.

The Examiner compares these registers within an I/O device to the "internal memory" as defined in the third paragraph of claim 16.

However, the Examiner is not correct when saying that Boettner discloses a memory configuration unit, being designed to make space for the peripheral device, on the one hand, and to make space from the internal memory not being made available to the peripheral device available for other data by access via an external bus. Importantly, registers in an I/O device are always reserved for this I/O device, irrespective of the fact whether this register is a privileged register or an unprivileged register. Any access to such a register of an I/O device will result in an activity of the I/O device. A read or write to an unprivileged register would, therefore, always result in a specific predetermined I/O action, as illustrated in column 5, lines 17-36 for the registers 400-405 of the I/O adaptor 410 in Fig. 10. Furthermore, it is emphasized that column 5, lines 62-64 clearly state that these registers are associated with an address in an unprivileged page and, are therefore, unprivileged registers.

In this respect, Boettner does not disclose that any internal memory is made available for any other devices connected to the bus. When Fig. 4 of Boettner is considered, then Boettner would have to shown that any of these registers in the I/O adaptor, which are not used for an I/O adapting action, could be used by any other

device for a completely different purpose. This, however, is not disclosed or rendered obvious in Boettner.

Furthermore, as correctly stated by the Examiner, it is to be emphasized that Boettner is silent about a volatile working memory having, on the one hand, an external working memory physically disposed outside the peripheral device and the available internal memory not assigned to the peripheral device, which is physically disposed within the peripheral device. This inside/outside feature is not disclosed in Boettner and is not at all mentioned by the Examiner. Instead, the Examiner simply ignored this feature in his statements under section 6 or 7 of the Office Action.

Regarding newly cited US 6,862,641 B1 (Strongin), hereinafter referred as Strongin, the Examiner points to Fig. 7a and 8. The Examiner simply asserts that memories 610A, 355 and 550 are "mapped" to each other. However, this would not make any sense, since nobody would map a secret register 610A to external memories, which are not as sensitive as the secret register 610A. Column 14, lines 1-23 also state in detail any memory address distributions. However, nothing is stated saying that 610A is mapped to the other memories.

Furthermore, all memories cited by the Examiner are ROM memories, which are read-only memories, which are, naturally, not any working memories, since a working memory, which is only implemented as a read-only memory would not make any sense. How can one work with a memory when one cannot write to this memory. Therefore the Examiner cannot assert that Strongin discloses a "register memory" or working memory and pointing to a read-only memory. Fig. 8A clearly states that all features are in an ROM and particularly a BIOS ROM, which is the basic input/output system read-only memory. Naturally, this has nothing to do with a volatile working memory, which is required for performing calculations and for writing to this memory. Contrary thereto, a ROM is never volatile. A ROM is always non-volatile.

Therefore, even when those skilled in the art would combine Boettner and Strongin, they would not have a device having the limitations as discussed above, with respect to Boettner. Instead, regarding claim 16, Strongin does not add anything, since an ROM cannot be compared to a working memory.

Applicants note that this amendment does not raise any new issues as the limitations added claims 1 and 9 were previously presented in claims 15 and 16.

Applicants have responded to all of the rejections and objections recited in the Office Action. Reconsideration and a Notice of Allowance for all of the pending claims are therefore respectfully requested.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

If the Examiner believes an interview would be of assistance, the Examiner is welcome to contact the undersigned at the number listed below.

Dated: February 8, 2007

Respectfully submitted,

By

Ian R. Blum

Registration No.: 42,336
DICKSTEIN SHAPIRO LLP
1177 Avenue of the Americas
New York, New York 10036-2714
(212) 277-6500
Attorney for Applicants

IRB/mgs